Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. Cancelled

2. (Currently Amended) The ~~PLL circuit according to claim 1,~~ A PLL circuit for use with first and second reference signals, with each reference signal having a phase, cycle, and frequency, and the cycle of the second reference signal being longer than that of the first reference signal, the PLL circuit comprising:

a voltage controlled oscillator for generating a clock signal in accordance with a control voltage, and the clock signal having a phase and frequency;

a first loop for controlling the frequency of the clock signal in accordance with the first reference signal; and

a second loop for controlling the phase of the clock signal in accordance with the second reference signal with the second loop generating the control voltage at a constant value and supplying the voltage controlled oscillator with the constant control voltage until the difference between the frequency of the first reference signal and the frequency of the clock signal converges to within a predetermined range, and thereafter the second loop generating the control voltage at a level in accordance with the difference between the phase of the second reference signal and the phase of the clock signal and supplying the voltage controlled oscillator with the control voltage at the level in accordance with said phase difference, wherein the second loop includes:

a voltage generation section for generating a plurality of constant control voltages having

different constant voltage values; and

a decoder for selecting one of the constant control voltages in accordance with a predetermined control signal, with the second loop supplying the voltage controlled oscillator with the constant control voltage selected by the decoder until the difference between the frequency of the first reference signal and the frequency of the clock signal converges to within the predetermined range.

3. (Currently Amended) The PLL circuit according to claim [[1]] 2, wherein the voltage controlled oscillator includes:

a first input terminal for receiving a first control voltage corresponding to the first loop;

a second input terminal for receiving a second control voltage corresponding to the second loop; and

a ring oscillator for generating the clock signal in accordance with the first and second control voltages;

the first loop generating the first control voltage at an amount in accordance with the difference between the frequency of the first reference signal and the frequency of the clock signal and applying the first control voltage to the first input terminal; and

the second loop generating the second control voltage at said level in accordance with the difference between the phase of the second reference signal and the phase of the clock signal and applying the second control voltage to the second input terminal.

4. (Currently Amended) The PLL circuit according to claim [[1]] 2, wherein the first loop includes:

a phase comparator for generating a comparison signal corresponding to the difference between the frequency of the first reference signal and the frequency of the clock signal; and

a charge pump connected to the phase comparator to control current in accordance with the comparison signal, the charge pump including a variable drive capacity and decreasing the drive capacity after the difference between the frequency of the first reference signal and the

frequency of the clock signal has been converged to within the predetermined range.

5. (Original) The PLL circuit according to claim 4, wherein the first reference and clock signals each have rising and trailing edges and the phase comparator includes:

a rising edge comparator for generating one signal in accordance with the difference between the timing of the rising edge of the first reference signal and the rising edge of the clock signal; and

a trailing edge comparator for generating another signal in accordance with the difference between the timing of the trailing edge of the first reference signal and the trailing edge of the clock signal;

the charge pump includes:

a first charge pump connected to the rising edge comparator; and

a second charge pump connected to the trailing edge comparator;

the first loop includes:

an adder connected to the first and second charge pumps to synthesize the outputs of the first and second charge pumps.

6. (Currently Amended) The PLL circuit according to claim [[1]] 2, wherein the first loop includes:

a first divisional circuit connected to the voltage controlled oscillator to divide the clock signal with a first dividing ratio and generate a first divisional clock signal having a frequency;

the second loop includes:

a second divisional circuit connected to the voltage controlled oscillator to divide the clock signal with a second dividing ratio and generate a second divisional clock signal having a phase, and the second loop supplies the voltage controlled oscillator with the constant control voltage until the difference between the frequency of the first reference signal and the frequency of the first divisional clock signal converges to within the predetermined range, and thereafter the second loop supplies the voltage controlled oscillator with the control voltage at the level in

accordance with the difference between the phase of the second reference signal and the phase of the second divisional clock signal.

7. (Original) The PLL circuit according to claim 6, wherein the second loop includes:

a phase comparator for generating a comparison signal corresponding to the difference between the phase of the second reference signal and the phase of the second divisional clock signal; and

a charge pump connected to the phase comparator to generate the control voltage at the level in accordance with the difference between the phase of the second reference signal and the phase of the second divisional clock signal, and the charge pump is inactivated until the difference between the frequency of the first reference signal and the frequency of the first divisional clock signal is converged to within the predetermined range.

8. Cancelled

9. (Currently Amended) ~~The data recording controller according to claim 8,~~ A data recording controller for generating a data write clock signal having a phase and frequency with a first signal indicating position information obtained from a disc medium, the rotation of which is controlled, and a second signal, the first and second signals each having a phase, cycle, and frequency, and the cycle of the second signal being longer than that of the first signal, the data recording controller including:

a voltage controlled oscillator for generating the clock signal in accordance with a control voltage;

a first loop for controlling the frequency of the clock signal in accordance with the first signal; and

a second loop for controlling the phase of the clock signal in accordance with the second signal, with the second loop generating the control voltage at a constant value and supplying the

voltage controlled oscillator with the constant control voltage until the difference between the frequency of the first signal and the frequency of the clock signal converges to within a predetermined range, and thereafter the second loop generating the control voltage at a level in accordance with the difference between the phase of the second signal and the phase of the clock signal and supplying the voltage controlled oscillator with the control voltage at the level in accordance with said phase difference, wherein the second loop includes:

a voltage generation section for generating a plurality of constant control voltages having different constant voltage values; and

a decoder for selecting one of the constant control voltages in accordance with a predetermined control signal, with the second loop supplying the voltage controlled oscillator with the constant control voltage selected by the decoder until the difference between the frequency of the first signal and the frequency of the clock signal converges to within the predetermined range.

10. (Currently Amended) The data recording controller according to claim [[8]] 9, wherein the voltage controlled oscillator includes:

a first input terminal for receiving a first control voltage corresponding to the first loop;

a second input terminal for receiving a second control voltage corresponding to the second loop; and

a ring oscillator for generating the clock signal in accordance with the first and second control voltages;

the first loop generating the first control voltage at an amount in accordance with the difference between the frequency of the first signal and the frequency of the clock signal and applying the first control voltage to the first input terminal; and

the second loop generating the second control voltage at said level in accordance with the difference between the phase of the second signal and the phase of the clock signal and applying the second control voltage to the second input terminal.

11. (Currently Amended) The data recording controller according to claim [[8]] 9, wherein the first loop includes:

a phase comparator for generating a comparison signal corresponding to the difference between the frequency of the first signal and the frequency of the clock signal; and

a charge pump connected to the phase comparator to control current in accordance with the comparison signal, wherein the charge pump has a variable drive capacity and decreases the drive capacity after the difference between the frequency of the first signal and the frequency of the clock signal is converged to within the predetermined range.

12. (Original) The data recording controller according to claim 11, wherein the first signal and clock signal each having rising and trailing edges and the phase comparator includes:

a rising edge comparator for generating one signal in accordance with the difference between the timing of the rising edge of the first signal and the rising edge of the clock signal; and

a trailing edge comparator for generating another signal in accordance with the difference between the timing of the trailing edge of the first signal and the trailing edge of the clock signal;

the charge pump includes:

a first charge pump connected to the rising edge comparator; and

a second charge pump connected to the trailing edge comparator;

the first loop includes:

an adder connected to the first and second charge pumps to synthesize the outputs of the first and second charge pumps.

13. (Original) The data recording controller according to claim 11, wherein the first loop includes:

a first divisional circuit connected to the voltage controlled oscillator to divide the clock signal and generate a first divisional clock signal having a frequency;

the second loop includes:

a second divisional circuit connected to the voltage controlled oscillator to divide the clock signal and generate a second divisional clock signal having a phase, and the second loop supplies the voltage controlled oscillator with the control voltage at the constant value until the difference between the frequency of the first signal and the frequency of the first divisional clock signal converges to within a predetermined range, and thereafter the second loop generates the control voltage at the level in accordance with the difference between the phase of the second signal and the phase of the second divisional clock signal and supplies it to the voltage controlled oscillator.

14. (Original) The data recording controller according to claim 13, wherein the second loop includes:

a phase comparator for generating a comparison signal corresponding to the difference between the phase of the second signal and the phase of the second divisional clock signal; and

a charge pump connected to the phase comparator to generate the control voltage at the level in accordance with the difference between the phase of the second signal and the phase of the second divisional clock signal, and the charge pump is inactivated until the difference between the frequency of the first reference signal and the frequency of the first divisional clock signal is converged to within the predetermined range.

15. Cancelled

16. (Currently Amended) ~~The method according to claim 15, further comprising:~~ A method for controlling a voltage controlled oscillator of a PLL circuit, the method comprising:

supplying the voltage controlled oscillator with a control voltage to generate a clock signal, which has a frequency and phase, in accordance with the control voltage;

controlling the frequency of the clock signal in accordance with a first signal having a frequency and cycle; and

controlling the phase of the clock signal in accordance with a second signal having a

phase and a cycle with the cycle of the second signal being longer than the cycle of the first signal;

wherein said controlling the phase of the clock signal includes:

generating the control voltage at a constant value and supplying the voltage controlled oscillator with the constant control voltage until the difference between the frequency of the first signal and the frequency of the clock signal converges to within a predetermined range; and

generating a voltage at a level in accordance with the difference between the phase of the second signal and the phase of the clock signal and supplying the voltage controlled oscillator with the voltage at the level in accordance with the phase difference after the difference between the frequency of the first signal and the frequency of the clock signal has been converged to within the predetermined range;

generating a plurality of constant control voltages having different constant voltage values; and

selecting one of the constant control voltages in accordance with a predetermined control signal; and

supplying the voltage controlled oscillator with the selected constant control voltage until the difference between the frequency of the first signal and the frequency of the clock signal is converged to within the predetermined range.

17. (Currently Amended) The method according to claim [[~~15~~]] 16, further comprising:

dividing the clock signal with a first dividing ratio to generate a first divisional clock signal having a frequency; and

dividing the clock signal with a second dividing ratio to generate a second divisional clock signal having a phase;

wherein said controlling the phase of the clock signal includes:

generating a control voltage at the constant value and supplying the voltage controlled

oscillator with the constant control voltage until the difference between the frequency of the first signal and the frequency of the first divisional clock signal is converged to within a predetermined range; and

generating the control voltage at the level corresponding to the difference between the phase of the second signal and the phase of the second divisional clock signal and supplying it to the voltage controlled oscillator after the frequency of the first signal and the frequency of the first divisional clock signal have been converged within the predetermined range.